UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/158,616	09/22/1998	HORMAZDYAR M. DALAL	F19-98-065	4171

32074 7590 08/28/2002

INTERNATIONAL BUSINESS MACHINES CORPORATION
DEPT. 18G
BLDG. 300-482
2070 ROUTE 52
HOPEWELL JUNCTION, NY 12533

EXAMINER
VIGUSHIN, JOHN B

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 08/28/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/158,616	DALAL ET AL.
	Examiner	Art Unit
	John B. Vigushin	2827

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 June 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7,9,10,12-33 and 35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,9,10,12,13,15-24,26-32 and 35* is/are rejected.

7)☒ Claim(s) *14,25 and 33* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 May 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. The present Office Action is responsive to Applicant's Amendment filed (faxed) June 13, 2002. The Examiner acknowledges the amendments to Claims 1 and 20, and the cancellation of Claims 11, 34 and 36-53. Accordingly, Claims 1-7, 9, 10, 12-33 and 35 remain pending in the instant amended Application.

Drawings

2. The new set of Formal Drawings filed on May 30, 2001 as Paper No. 13 incorporate the Applicant's correction to Fig. 7 (see Paper No. 4) and have been approved by the Official Draftsman.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claim 35 is rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. In lines 5-8 of the claim, the Applicant recites, "wherein the third circuitized card is electrically connected to the second interposer through a **fourth** set of connections, and wherein the second interposer is electrically connected to the second circuitized card through a **fourth** set of connections" (bold emphasis by the

Examiner). Having the above two connections evidently performed by **the same (fourth)** set of connections renders the claim non-enabling. **The rejection may be overcome by simply changing "fourth" to --fifth-- in line 8 (i.e., the last line) of the claim**. This modification of the claim language is the one the Examiner will use to reject Claim 35 over the prior art, below.

Rejections Based On Prior Art

5. The following references were relied upon for the rejections hereinbelow:

Saito et al. (US 5,570,274)* Wang (US 6,344,688 B1)

*Already made of record in the instant Application.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-7, 9, 10, 12, 13, 15-24, 26-32 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Saito et al. in view of Wang.

As to Claim 1:

I. Saito et al. discloses, in Fig. 9: a package for containing electronic components, the package comprising: a first (upper) circuitized card 1 and a second (lower) circuitized card 1 (Fig. 9); an interposer (the two elements 4 joined at bumps 11,

as shown in Fig. 9, hereinafter referred to as "the interposer"; see the Examiner's annotated version of Fig. 9 in Saito et al., labeled ***Exhibit A***, attached to the present Office Action) interposed between the first and second circuitized cards 1 (Fig. 9); the interposer comprising a circuitized card (Fig. 3B; col.3: 13-17) and having an opening (Fig. 3A), the opening of the interposer and the first and second circuitized cards 1 forming a cavity for containing at least one electronic component 2 (Fig. 9: the cavity is represented by the space between circuitized cards 1 where components 2 are mounted); wherein the first circuitized card 1 (upper card 1) has a bottom surface and there is at least one component 2 mounted to the bottom surface (Fig. 9).

II. Saito et al. discloses that the first and second circuitized cards 1 are circuitized organic or inorganic cards (col.8: 39-40). However, Saito et al. is silent as to the material composition of the frame and is silent concerning the structure of the organic cards 1 and interposer, i.e., whether or not the organic cards 1 and interposer have a multilayer laminate structure (however, such a multilayer structure for circuitized card 1 is disclosed for the embodiment in Fig. 5 having no discrete interposer).

III. Wang discloses a substrate (Fig. 8; flexible substrate 10) made of polyimide material for the purpose of reducing the profile of the substrate, hence also of the package (col.2: 30-39; col.3: 33 and 48-50). Wang also discloses that substrate 10 is a multilayer laminate substrate (Figs. 2, 3A,B and 8; col.3: 60-64). Wang further discloses a multilayer laminate interposer substrate 60 with cavity 64 (Figs. 5, 6, 7 and 8; col.4: 35-46) wherein the multilayer interposer 60 includes ground and power planes 70 and 72 for connection to the components 18, 20 in the cavity 64. Wang does not indicate

the material composition of the interposer 60 but teaches that it too is fabricated to have a low profile (col.4: 49-50) enabling a low packaging profile for the finished assembly (col.4: 63-65).

IV. Since Wang requires a finished package assembly having a low profile, and since organic substrates (e.g., polyimides) are taught by Wang as capable of being fabricated with small thicknesses, then it would have been obvious to one of ordinary skill in the art at the time of the invention to use an organic material, such as a polyimide, for the interposer 60 since such materials can be fabricated with small thicknesses in order to achieve a low packaging profile for the finished assembly.

V. Furthermore, low packaging profiles are of the utmost utility as taught by Wang (col.2: 30-35). Since both Saito et al. and Wang are both in the art of high density multichip module packaging and, since Saito et al. also recognizes the need in industry to accommodate as much electronic functionality as possible in a compact package (Saito et al., col.1: 43-54), the utility of multilayer laminate packaging using organic materials would have been readily recognized in the pertinent art of Saito et al. wherein the multilayer circuitry enables power/ground planes and increased circuit and routing densities in the small and low-profile-substrate dimensional constraints required by miniaturized electronics applications (cell phones, pagers, laptops, etc.), and the organic material compositions lend themselves to enabling the low (thin) packaging profiles required by those applications.

VI. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the circuitized cards 1 of Saito et al. with the

circuitized organic multilayer laminate substrate 10 of Wang, and to modify the interposer of Saito et al. with the circuitized organic multilayer laminate interposer 60 of Wang in order to enable a high density multichip module in Saito et al. that has a high density of functional electronics in a compact package that includes the feature of a low packaging profile useful for miniaturized electronic components such as cell phones, pagers, laptops, etc., as taught by Wang.

As to Claim 2, modified Saito et al. discloses that the interposer, first circuitized card 1 and second circuitized card 1 form--by means of bottom and side terminals 5 and 7, and bumps 11 (see Figs. 3B and 9)--a metallic enclosure that inherently acts as a Faraday shield for electronic components placed inside the cavity (Saito et al.: Fig. 9); moreover, the interposer of Saito et al. as modified, above, by the interposer 60 of Wang has ground and power planes 70 and 72 connected to metallic vias embedded within the interposer and connected to connections 76 (Wang: Fig. 8; col.42-46) which inherently provide a Faraday shield for the components in the cavity.

As to Claim 3, modified Saito et al. discloses that the interposer, as modified above by Wang, has at least one connection 11 to at least one ground by means of a ground plane (see Wang: connection 76--corresponding to connection 11 of Saito et al.--and ground plane 70 in Fig. 8; col.4: 42-46).

As to Claim 4, modified Saito et al., as modified, above, by Wang, further discloses a multiplicity of such connections to the at least one ground, the distance between a connection and its closest neighboring connection being approximately equal (Wang: see connections 76 in Fig. 7; Saito et al.: see connections 11 in Fig. 3A).

As to Claim 5, modified Saito et al. discloses that the opening is square and is in the approximate center of the interposer 4 (Saito et al.: Fig. 3A).

As to Claim 6, modified Saito et al. discloses that the interposer is electrically and physically connected to the first and second circuitized cards 1 (Saito et al.: Fig. 9).

As to Claim 7, modified Saito et al. discloses that the first (upper) circuitized card 1 has a top surface having at least one component 2 mounted thereto (Saito et al.: Fig. 9).

As to Claim 9, modified Saito et al. discloses that the second (lower) circuitized card 1 has a top surface having at least one component 2 mounted thereto (Saito et al.: Fig. 9).

As to Claim 10, modified Saito et al. discloses that the second (lower) circuitized card 1 has a bottom surface having at least one component 2 mounted thereto (Saito et al.: Fig. 9).

As to Claim 12, modified Saito et al. discloses that the second (lower) circuitized card 1 has a bottom surface and the bottom surface has a ball grid array 11 (provided by the lower interposer 4 **on the bottom surface** of second circuitized card 1) allowing connection to a system board 10 (Saito et al.: Fig. 9).

As to Claim 13, modified Saito et al. discloses that the first circuitized card and interposer are connected through surface mount technology and the second circuitized card 1 and interposer are connected through surface mount technology (Saito et al.: Fig. 9).

As to Claim 15, modified Saito et al. discloses that first (upper) circuitized card 1 has a top surface, the second (lower) circuitized card 1 has a top surface and a bottom surface, and there is at least one component 2 on the top surface of first circuitized card 1, and there is at least one component 2 on the top surface of second circuitized card 1 (Saito et al.: Fig. 9).

As to Claim 16, modified Saito et al. teaches all the limitations of the claim except that the at least one component 2 is attached to a heat sink. However, heat sinks attached to electronic components such as components 2 are notorious in the electronics packaging art and therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide a heat sink for at least one component 2 in order to draw off the heat generated during device operation.

As to Claim 17, modified Saito et al. discloses that the cavity contains at least one component 2 (Saito et al.: Fig. 9).

As to Claim 18, modified Saito et al. discloses that the at least one component inside the cavity is attached to a bottom surface of the first (upper) circuitized card 1 through surface mount (flip-chip) attachment (Saito et al.: Fig. 9; col.5: 17-19).

As to Claim 19, modified Saito et al. discloses that the first (upper) circuitized card 1 has a top surface and at least one component 2 mounted thereto through surface mount (flip-chip) attachment (Saito et al. Fig. 9; col.5: 17-19).

As to Claim 20:

I. Saito et al. discloses, in Fig. 9: a first (upper) circuitized card 1 having a top and bottom surface; a second (lower) circuitized card 1 having a top and bottom

surface; an interposer (the two elements 4 joined at bumps 11, as shown in Fig. 9, hereinafter referred to as "the interposer") having an opening (Fig. 3A), a top surface and a bottom surface; the interposer being electrically connected to first and second circuitized cards 1 through a first and second set of connections (solder joints 8; see Figs. 3B and 9); the bottom surface of the second (lower) circuitized card 1 has a third set of connections--i.e., solder joints 8 in conjunction with lower circuitized interposer 4 mounted to the bottom surface of the second (lower) circuitized card 1--for attaching the second circuitized card to a system card 10 (Fig. 9); the opening in the interposer, the bottom surface of first (upper) circuitized card 1 and the top surface of second (lower) circuitized card 1 form a cavity for containing at least one electronic component 2 (Fig. 9).

IIa. Saito et al. does not teach, in the embodiment of Fig. 9, that the first set of connections (solder joints 8) are interposed between the bottom surface of first (upper) circuitized card 1 and the top surface of the interposer; and does not teach that the second set of connections (solder joints 8) are interposed between the bottom surface of the interposer and the top surface of second (lower) circuitized card 1. Since the layout of the first and second circuitized cards 1 requires pads 3 at the periphery of first and second circuitized cards 1 (see Figs. 3A,B and 9), the first and second sets of connections (i.e., solder joints 8) are established between the *side terminals* 7 of the interposer and the pads 3 on the bottom surface of the first (upper) circuitized card 1, and between the *side terminals* 7 of the interposer and the pads 3 on the top surface of the second (lower) circuitized card 1 (Fig. 9).

IIb. However, Saito et al. does teach an embodiment (Fig. 4) wherein a circuitized card 1 requires a layout of pads 35 around the periphery of the bottom surface of card 1 such that an interposer 4 is connected to the circuitized card 1 by means of a set of connections (solder joints 12) interposed between the top surface (comprising terminal 36) of the interposer 4 and the bottom surface of card 1.

IIc. Since it is clear that the manner of connection between interposer and cards 1 depends on the circuit routing and pad layout of the cards 1, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the circuit routing and contact pad layout of the first and second circuitized cards 1 of the Fig. 9 embodiment with the circuit routing and contact pad layout of circuitized card 1 of the Fig. 4 embodiment in applications where the circuit routing and pad layout of the Fig. 4 embodiment are electronically required by an application using the stacked structure of the Fig. 9 embodiment, wherein, consequently, the first set of connections (solder joints) are then interposed between the bottom surface of first (upper) circuitized card 1 and the top surface of the interposer, and the second set of connections (solder joints) are interposed between the bottom surface of the interposer and the top surface of second (lower) circuitized card 1, as taught in the embodiment of Fig. 4.

IIIa. Saito et al. discloses that the first and second circuitized cards 1 are circuitized organic or inorganic cards (col.8: 39-40). However, Saito et al. is silent as to the material composition of the frame and is silent concerning the structure of the organic cards 1 and interposer, i.e., whether or not the organic cards 1 and interposer

have a multilayer laminate structure (however, such a multilayer structure for circuitized card 1 is disclosed for the embodiment in Fig. 5 having no discrete interposer).

IIIb. Wang discloses a substrate (Fig. 8; flexible substrate 10) made of polyimide material for the purpose of reducing the profile of the substrate, hence also of the package (col.2: 30-39; col.3: 33 and 48-50). Wang also discloses that substrate 10 is a multilayer laminate substrate (Figs. 2, 3A,B and 8; col.3: 60-64). Wang further discloses a multilayer laminate interposer substrate 60 with cavity 64 (Figs. 5, 6, 7 and 8; col.4: 35-46) wherein the multilayer interposer 60 includes ground and power planes 70 and 72 for connection to the components 18, 20 in the cavity 64. Wang does not indicate the material composition of the interposer 60 but teaches that it too is fabricated to have a low profile (col.4: 49-50) enabling a low packaging profile for the finished assembly (col.4: 63-65).

IIIc. Since Wang requires a finished package assembly having a low profile, and since organic substrates (e.g., polyimides) are taught by Wang as capable of being fabricated with small thicknesses, then it would have been obvious to one of ordinary skill in the art at the time of the invention to use an organic material, such as a polyimide, for the interposer 60 since such materials can be fabricated with small thicknesses in order to achieve a low packaging profile for the finished assembly.

IIId. Furthermore, low packaging profiles are of the utmost utility as taught by Wang (col.2: 30-35). Since both Saito et al. and Wang are both in the art of high density multichip module packaging and, since Saito et al. also recognizes the need in industry to accommodate as much electronic functionality as possible in a compact

package (Saito et al., col.1: 43-54), the utility of multilayer laminate packaging using organic materials would have been readily recognized in the pertinent art of Saito et al. wherein the multilayer circuitry enables power/ground planes and increased circuit and routing densities in the small and low-profile-substrate dimensional constraints required by miniaturized electronics applications (cell phones, pagers, laptops, etc.), and the organic material compositions lend themselves to enabling the low (thin) packaging profiles required by those applications.

IIIe. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the circuitized cards 1 of Saito et al. with the circuitized organic multilayer laminate substrate 10 of Wang, and to modify the interposer of Saito et al. with the circuitized organic multilayer laminate interposer 60 of Wang in order to enable a high density multichip module in Saito et al. that has a high density of functional electronics in a compact package that includes the feature of a low packaging profile useful for miniaturized electronic components such as cell phones, pagers, laptops, etc., as taught by Wang.

As to Claim 21, modified Saito et al. discloses that the cavity contains at least one electronic component 2 (Saito et al.: Figs. 3A and 9).

As to Claim 22, modified Saito et al. discloses at least one component inside the cavity is attached to a bottom surface of the first (upper) circuitized card 1 through surface mount (flip-chip) attachment (Saito et al.: Fig. 9; col.5: 17-19).

As to Claim 23, modified Saito et al. discloses that first (upper) circuitized card 1 has a top surface and at least one component 2 mounted thereto through surface mount (flip-chip) attachment (Saito et al.: Fig. 9; col.5: 17-19).

As to Claim 24, modified Saito et al. discloses that each set of the first, second and third sets of connections is a plurality of surface mount connections (Saito et al.: Fig. 9).

As to Claim 26, modified Saito et al. discloses that the interposer forms--by means of bottom and side terminals 5 and 7, and bumps 11 (see Figs. 3B and 9)--a metallic enclosure that inherently acts as a Faraday shield for electronic components placed inside the cavity (Saito et al.: Fig. 9); moreover, the interposer of Saito et al. as modified, above, by the interposer 60 of Wang has ground and power planes 70 and 72 connected to metallic vias embedded within the interposer and connected to connections 76 (Wang: Fig. 8; col.42-46) which inherently provide a Faraday shield for the components in the cavity.

As to Claim 27, modified Saito et al. discloses that the interposer, as modified above by Wang, has at least one connection 11 to at least one ground by means of a ground plane (see Wang: connection 76--corresponding to connection 11 of Saito et al.--and ground plane 70 in Fig. 8; col.4: 42-46).

As to Claim 28, modified Saito et al., as modified, above, by Wang, further discloses a multiplicity of such connections to the at least one ground, the distance between a connection and its closest neighboring connection being approximately equal (Wang: see connections 76 in Fig. 7; Saito et al.: see connections 11 in Fig. 3A).

As to Claim 29, modified Saito et al. discloses that the opening is rectangular and in the approximate center of the interposer (Fig. 3A).

As to Claim 30, modified Saito et al. discloses at least one electronic component 2 mounted to the top surface of the first (upper) circuitized card 1 (Saito et al.: Fig. 9).

As to Claim 31, modified Saito et al. discloses at least one electronic component 2 mounted to the bottom surface of the first (upper) circuitized card 1 (Saito et al.: Fig. 9).

As to Claim 32, modified Saito et al. discloses at least one electronic component 2 mounted to the top surface of the second (lower) circuitized card 1 (Saito et al.: Fig. 9).

As to Claim 35:

I. Modified Saito et al. teaches all the limitations of base Claim 20 in the embodiment of Fig. 9 but does not teach, in the Fig. 9 embodiment, a third circuitized card and a second interposer having a second opening, wherein the third circuitized card, second (lower) circuitized card 1, and the second opening in the second interposer define a second cavity for containing at least one electronic component 2, wherein the third circuitized card is electrically connected to the second interposer through a fourth set of connections, and wherein the second interposer is electrically connected to the second (lower) circuitized card 1 through a fifth set of connections.

II. Modified Saito et al. teaches the above "double-deck" structure in order to increase the number of components 2 or at least double the packaging density (col.9: 34-36). Since the point of the Fig. 9 embodiment is to teach that stacking is another

way of increasing packaging density and circuit functionality, it would have been obvious to one of ordinary skill in the art at the time the invention was made to add yet another (i.e., third) circuitized card 1 with interposer 4--utilizing the structure of the Fig. 3B or Fig. 4 embodiments--to the stacked configuration of the Fig. 9 embodiment (see the modification of Fig. 9 in the Examiner's ***Exhibit B*** drawing attached to the present Office Action), the third circuitized card 1 and a second interposer 4 having a second opening (Fig. 3A), wherein the third circuitized card 1, second (lower) circuitized card 1, and the second opening in the second interposer 4 define a second cavity for containing at least one electronic component 2, wherein the third circuitized card 1 is electrically connected to the second interposer 4 through a fourth set of connections (solder joints 8), and wherein the second interposer 4 is electrically connected to the second (lower) circuitized card 1 through a fifth set of connections: i.e., solder bumps 11 of second interposer 4, in conjunction with the solder bumps 11, the terminals of the lower interposer 4 and solder joints 8 electrically connected to the bottom surface of second (lower) circuitized card 1. Thus, even greater circuit functionality and packaging density can be realized.

Allowable Subject Matter

8. Claims 14, 25 and 33 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

9. The following is a statement of reasons for the indication of allowable subject matter:

As to Claim 14, patentability resides in that *the interposer and first circuitized card are connected through a ball grid array and the interposer and the second circuitized card are connected through a ball grid array*, in combination with the other limitations of the claim.

As to Claim 25, patentability resides in that *each set of connections of the first, second and third sets of connections is a ball grid array*, in combination with the other limitations of the claim.

As to Claim 33, patentability resides in that *the interposer has at least one electronic component on its surface*, in combination with the other limitations of the claim.

10. As allowable subject matter has been indicated, applicant's reply must either comply with all formal requirements or specifically traverse each requirement not complied with. See 37 CFR 1.111(b) and MPEP § 707.07(a).

Response to Applicant's Remarks

11. The indication of patentability of the subject matter in canceled Claims 11 and 34, as incorporated into base Claims 1 and 20, respectively, has been withdrawn in view of new prior art.

12. The reliance on Saito et al. in the above rejections has been rendered in greater detail than in the rejections over Saito et al. in the previous Office Action.

Conclusion

13. **Due to changes in the Office the present Examiner has replaced Examiner David A. Foster as the Examiner of record.** Accordingly, any inquiry concerning this communication or earlier communications from the examiner should be directed to John B. Vigushin whose telephone number is 703-308-1205. The examiner can normally be reached on 8:30AM-5:00PM Mo-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David L. Talbott can be reached on 703-305-9883. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7382 for regular communications and 703-308-7382 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

John B. Vigushin
Examiner
Art Unit 2827

jbv
August 24, 2002

KAMAND CUNEO
PRIMARY EXAMINER

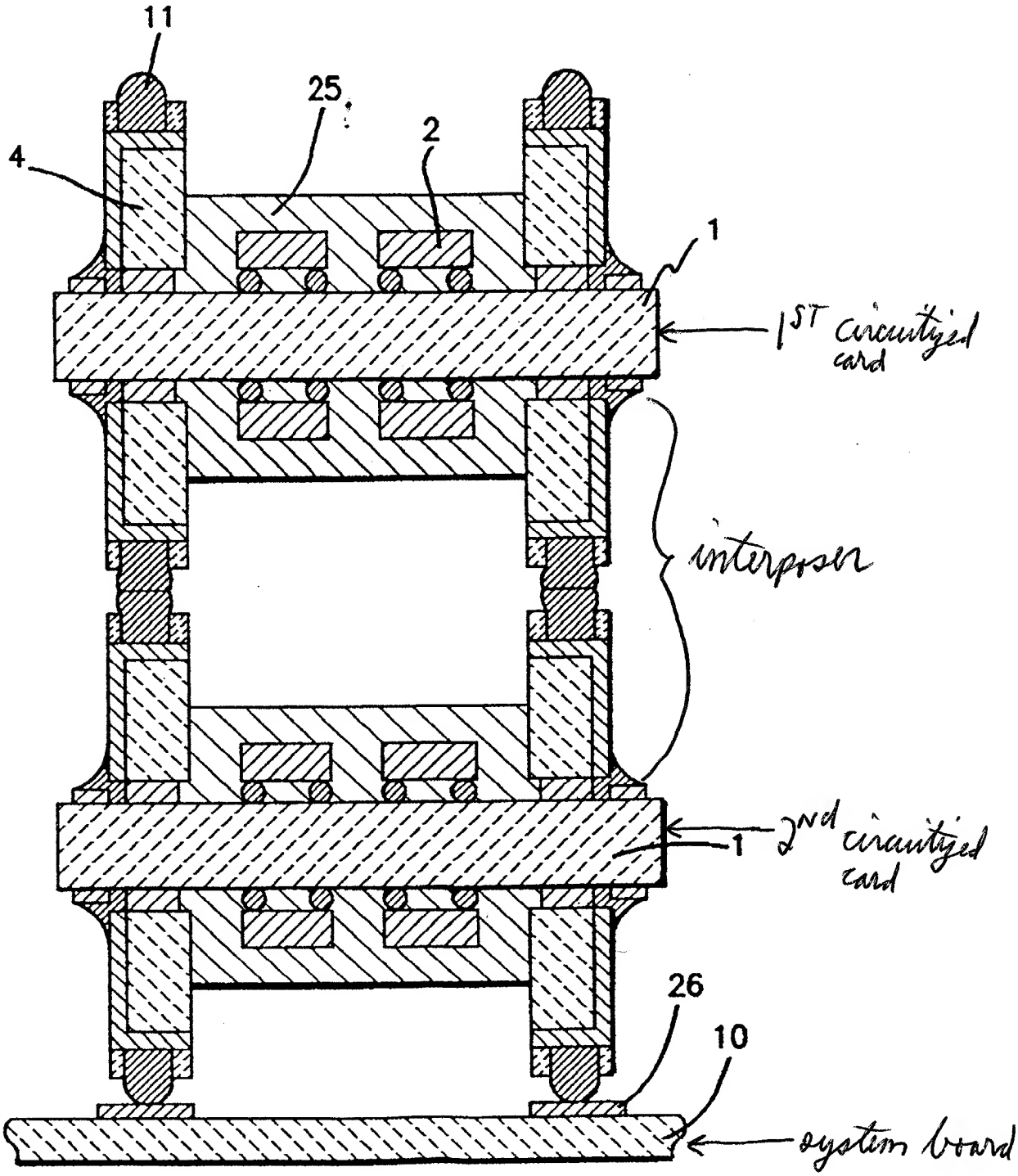

FIG. 9 (Examiner's Annotated Version)

EXHIBIT A

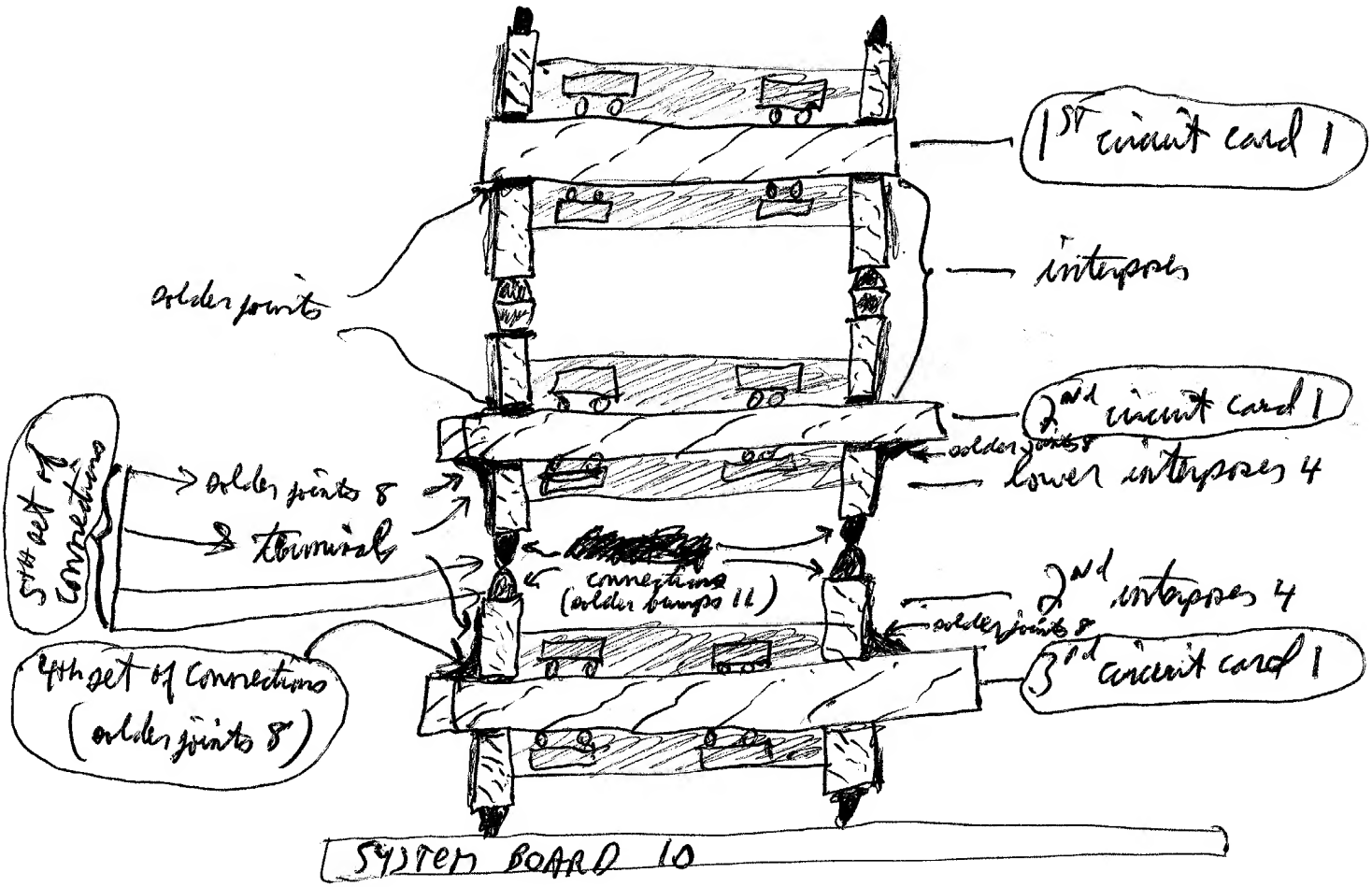

EXHIBIT B

Obvious modification of the embodiment of Fig. 9 in Saito et al. (US 5,570,274) for the rejection of claim 35.